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PATENT APPLICATION
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JOSEPH S. MAKUCH (SENDER'S PRINTED NAME)

Joseph S. Makuch (SIGNATURE)

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Enclosed for filing is a patent application under 37 CFR 1.53(b) of:

Inventor: Barrie Gilbert
For: GAIN AND PHASE DETECTOR HAVING DUAL LOGARITHMIC AMPLIFIERS

Enclosures:
☒ Specification (pages 1-8); claims (pages 9-12); abstract (page 13)
☒ 5 sheet(s) of INFORMAL drawings
☒ Declaration or Combined Declaration and Power of Attorney (unsigned)
☒ Return Postcard

CLAIMS AS FILED				
For	Number Filed	Number Extra	Rate	Basic Fee $690
Total Claims	27-20	7	x $ 18 =	$126
Independent Claims	4-3	1	x $ 78 =	$78
Multiple Dependent Claim Fee			x $260 =	
TOTAL FILING FEE				$894

Respectfully submitted,

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GAIN AND PHASE DETECTOR HAVING DUAL LOGARITHMIC AMPLIFIERS

This application claims priority from U.S. Provisional Application No. 60/231,505 titled Gain And Phase Detector Having Dual Logarithmic Amplifiers filed September 9, 2000 which is incorporated by reference.

BACKGROUND OF THE INVENTION

Fig. 1 illustrates a chain of gain stages 2 for a prior art logarithmic amplifier (log amp). A series of detector cells 4 combine the outputs from the gain stages to generate a logarithmic output V_{OUT}. The gain stages are typically implemented as limiting amplifiers having the form A/0. That is, for small inputs, the gain stages have an incremental gain of A, but at a certain point, the output is limited, and the incremental gain becomes zero as shown in Fig. 2. The response of the system of Fig. 1 is:

$$V_{OUT} = V_y \log\left(\frac{V_{IN}}{V_x}\right) \qquad \text{(Eq. 1)}$$

where V_y and V_x are parameters that are built into the system and define its calibration. Referring to Fig. 3, V_y scales the slope, and V_x is the intercept along the horizontal axis. The intercept is usually an extrapolated parameter because in practice, it is unlikely that the output will drop below the nose floor as shown with the broken line in Fig. 3. Both V_x and V_y may be temperature dependent, and must therefore be temperature compensated to maintain the accuracy of the log amp. These are matters that have received close attention in prior invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram of a prior art logarithmic amplifier.

Fig. 2 illustrates the incremental gain for a limiting amplifier used as gain stage in the logarithmic amplifier of Fig. 1.

Fig. 3 illustrates the output characteristic of the logarithmic amplifier of Fig. 1.

Fig. 4 illustrates an embodiment of a detector in accordance with the present invention.

Fig. 5 illustrates another embodiment of a detector in accordance with the present invention.

Fig. 6 illustrates the layout of an embodiment of a detector having co-integrated logarithmic amplifier in accordance with the present invention.

Fig. 7 illustrates generally the packaging parasitics associated with a practical embodiment of a detector in accordance with the present invention.

Fig. 8 illustrates the frequency response of each channel taken separately of an embodiment of a detector in accordance with the present invention.

Fig. 9 illustrates another embodiment of a detector in accordance with the present invention.

DETAILED DESCRIPTION

The present invention utilizes two logarithmic amplifiers (log amps) coupled to circuitry that processes the outputs from the log amps in one or more ways to perform useful functions. For example, in one aspect of the present invention, taking the difference of the logarithmic outputs from the log amps eliminates the intercept V_x as a parameter when measuring the ratio of two signals, which could correspond to a system gain or loss. In another aspect of the present invention, a phase detector core can be utilized to measure the relative phase of two signals that are applied to the log amps. In a preferred embodiment, the two log amps are co-integrated as a single integrated circuit to create a combined gain-phase detector that can be described as a network analyzer on a chip. The present invention, however, is not limited to any specific embodiment, and it should be apparent that, although the principles of the present invention will be described with reference to some example embodiments illustrated below, the present invention can be modified in arrangement and detail without departing from such principles.

As mentioned above, one aspect of the present invention involves differentially processing the logarithmic outputs from two log amps. An embodiment of a circuit that performs this function is illustrated in Fig. 4. The circuit of Fig. 4 includes a first log amp 10, a second log amp 12, and a differencing circuit 14. Each of the log amps includes a series of gain stages 16, which in this example, are limiting amplifiers having the form A/0 as shown in Fig. 2. The use of limiting amplifiers is not essential to the present invention, but they provide convenient hard-limited output signals which are especially useful for measuring phase as

described below. Each log amp also includes detector cells 18 which combine the outputs from the gain stages to generate a logarithmic output.

Log amp 10 will be referred to as part of channel A, which receives the input signal V_A and generates the logarithmic output signal V_{OUT_A}. Likewise, log amp 12 will be referred to as part of channel B, which receives the input signal VB and generates the logarithmic output signal V_{OUT_B}. For purposes of illustration, the signals utilized in Fig. 4 are shown as single-sided voltages, but the present invention can be realized with differential voltage signals, differential or single-sided current mode signals, or any convenient combination thereof. The logarithmic output signals V_{OUT}_A and V_{OUT_B} are given by the following equations:

$$V_{OUT\_A} = V_y \log\left(\frac{V_A}{V_x}\right) \qquad \text{(Eq. 2)}$$

$$V_{OUT\_B} = V_y \log\left(\frac{V_B}{V_x}\right) \qquad \text{(Eq. 3)}$$

The differencing circuit 14 processes the logarithmic signals differentially so that the output signal V_{OUT} is given by the difference of two logarithms:

$$V_{OUT} = V_{OUT\_A} - V_{OUT\_B} = V_y \log\left(\frac{V_A}{V_B}\right) \qquad \text{(Eq. 4)}$$

Thus, the intercept V_x, which depends on the particulars of the design of the log amps, and which is prone to error, is completely eliminated as a parameter. The output is simply proportional to the logarithm of V_A/V_B, with V_y setting the slope. Therefore, there is no need to temperature compensate the intercept. Moreover, since the system response is ratiometric with respect to V_A and V_B, it allows gain to be measured directly. For example, if the V_A and V_B inputs are connected to the input and output ports of a power amplifier, the output V_{OUT} provides a measure of the gain of the power amplifier. Normally, gain is measured by measuring the absolute power or voltage at the input port,.taking another absolute measurement at the output port, and then performing a computation by hand or with a microprocessor. With the present invention, however, the absolute magnitudes do not matter since the response is entirely ratiometric. A further advantage of the system of Fig. 4 is that it tends to cancel aberrations in

the frequency responses of the individual log amps, thereby extending the effective frequency response of the entire system. These and other advantages will be explained in more detail below.

The present invention also contemplates a method for utilizing two log amps as shown in Fig. 4 as an accurately calibrated log amp having an absolute intercept by indirect means. This can be achieved by applying the signal to be measured to the more accurate V_A input and a reference signal to the V_B input. This eliminates the need for precision internal intercept calibration and transfers it to an external source where it is easier to generate a very accurate reference signal. For example, if the reference signal is an AC excitation having the same waveform (most usually sinusoidal) as the signal to be examined, an absolute AC based intercept is achieved.

The present invention also contemplates many variations to the system shown in Fig. 4. For example, the differencing circuit can modified to add or subtract the outputs from the log amps at will to produce a continuous product, a continuous quotient, a mixture of products and quotients, etc. This is especially easy if the log amps are implemented with differential current outputs which can be added or subtracted using simple wire connections as summing nodes. Moreover, although the embodiment of Fig. 4 only includes two log amps, a system in accordance with the present invention can utilize any number of log amps to provide additional functionality, such as the product of three, four, or more RF signals as shown in Fig. 9.

Even more additional techniques are contemplated by the present invention. For example, two sinusoidal signals can be applied to the V_A and V_B inputs to perform division from high frequency (HF) down to base band. If the amplifiers are DC coupled, then a DC signal can be applied to the V_B input to set a DC intercept. Alternatively, if a DC signal is applied to the V_A input, and a wide dynamic range signal is applied to the V_B input, the polarity of the response is inverted, resulting in a hyperbolic response. The methods contemplated by the present invention, however, are not limited to DC or sinusoidal waveforms. For example, one particularly interesting technique involves the use of a two log amp system according to the present invention with a base station that utilizes a code division multiple access (CDMA) transmission scheme. If a modulated CDMA signal having a complex structure is applied to the V_A input, and the modulation waveform from the base band portion of the system is applied to the V_B input, then the modulated signal is divided by its own modulation waveform. Thus, there

is essentially an instantaneous division of a modulated RF carrier by the very modulation imposed on it. This results in an immediate analog computation of the RF power, without having to wait for the response lag of the low-pass filter conventionally required to remove fluctuations due to the modulation. Thus, a two log amp system in accordance with the present invention can be used as both an in-line processor for high volume applications such as handsets, as well as in high performance base stations as a system monitoring tool and power controller for advanced linearization techniques now in use.

Another, separable, aspect of the present invention involves the use of a phase detector core to measure the relative phase of two signals applied to the log amps as illustrated in Fig. 5. The system of Fig. 5 includes channel A and channel B log amps which are implemented with limiting amplifiers as in Fig. 4. However, rather than utilizing the logarithmic outputs V_{OUT_A} and V_{OUT_B}, the system of Fig. 4 utilizes the limiting outputs V_{LIM_A} and V_{LIM_B} from the last limiting amplifier in each log amp, which are typically almost perfect, hard-limited square waves. The phase relationship between the two input signals V_A and V_B is embedded in the limiting outputs. A phase detector core 20, which is preferably implemented as a multiplier, processes the limiting outputs to generate a phase output V_{PHASE} that provides a calibrated measure of the phase between V_A and V_B.

The phase detector core of Fig. 5 can be added to the system of Fig. 4 to create a system that simultaneously measures both the gain and phase of the two input signals V_A and V_B applied to the log amps. This creates a neatly interconnected arrangement because the differencing circuit utilizes the logarithmic outputs of the log amps, while the phase detector core utilizes the limiting outputs which are generated as a byproduct in log amps that utilize limiting amplifiers as the gain stages. The inputs V_A and V_B can be coupled to two points of interest in a signal path or a system under test, and the gain and phase can be measured simultaneously. Although there are many different situations in which it is important to measure gain and phase, it is particularly useful in connection with modern power amplifiers used in base stations for wireless communications. The outputs from a gain-phase detector in accordance with the present invention can be fed back to the communication system which can then affect some signal processing to minimize distortion.

In a preferred embodiment, two log amps in accordance with the present invention are co-integrated into a single integrated circuit (IC) as shown in Fig. 6. The circuit of Fig. 6 is

fabricated on a substrate (chip) 21 which is bisected by a center line "C/L". The channel A log amp 10 is located on the top half of the chip, while the channel B log amp 12 is formed on bottom half of the chip opposite the channel A log amp. The phase detector core 20 is located on the center line between the log amps, as is a bias circuit 22. A gain output interface circuit 24 and a phase output interface circuit 26 are located next to the channel A and B log amps, respectively, and on opposite sides of the center line. Filter capacitors 28 are also located symmetrically on opposite sides of the center line. The components are accessed through bond pads 30 symmetrically disposed around the chip.

For ease of illustration, the components in Fig. 6 are shown utilizing single-sided signals, but in a practical embodiment, the signals would preferably be implemented as fully differential signals as is typical with integrated circuits. The gain stages in the log amps 10 and 12 are preferably implemented as limiting amplifiers such as those disclosed in U.S. Patent Application Ser. No. 09/241,359 titled "Logarithmic Amplifier With Self-Compensating Gain For Frequency Range Extension" filed January 29, 1999 by the same inventor as the present application, and which is herein incorporated by reference.

The phase detector core 20 is preferably a four-transistor multiplier such as the one disclosed in U.S. Patent Application Ser. No. 09/473,309 filed December 28, 1999 titled RMS-DC Converter Having Gain Stages With Variable Weighting Coefficients by the same inventor as the present application, and which is incorporated by reference. By adjusting the tail current through the multiplier, the scale factor of the phase output PHASE can be adjusted.

The gain output interface 24 includes a differencing circuit that generates the difference in the logarithmic outputs from the log amps. If the phase detector core is implemented with a circuit that generates a fully differential output signal, then the phase output interface circuit 26 should also preferably include a differencing circuit to convert the differential output from the phase detector core to a single-sided signal. Both the gain output interface 24 and the phase output interface circuit 26 preferably include rail-to-rail output buffers that provide single-sided output signals GAIN and PHASE having the widest possible voltage range for a given supply voltage.

The bias circuit 22 generates bias signals that used for biasing the various components of the system of Fig. 6 and to set the slope of the log amps 10 and 12.

Filter capacitors 28 provide independent high frequency filtering for both the gain and phase outputs, and the capacitor connections are preferably brought outside of the chip package through bond pads so that external capacitors can be added to extend the filtering time constants for both gain and phase.

One advantage of co-integrating two log amps into a single integrated circuit in accordance with the present invention is that it allows for cancellation of packaging parasitics. For example, the IC chip 21 of Fig. 6 would typically be mounted in a package having terminal pins that are connected to the bond pads by bondwires. The bondwires and pins have inductances, and there are typically stray capacitances associated with the pins, bond pads and bondwires. These parasitic reactances are shown generically in Fig. 7 as networks 34 coupled between pins 36 and bond pads 30 on the chip 21. Each of the networks has a general frequency response that can be denoted by h(s), where s is the complex frequency. By observing careful symmetry in the layout of the chip (which is generally symmetric about the center line C/L in Fig. 6) and the disposition of the chip within the package, the frequency behavior of both of the networks 34 are identical, so their effects cancel in the ratio. Thus, a symmetrically designed system in accordance with the present invention also eliminates measurement uncertainties arising from packaging parasitics.

A further advantage of the present invention can be understood by first considering the frequency response of each log amp as a stand-alone element having a frequency response g(s). The combined of each log amp and its respective parasitic network 34 is h(s)•g(s) as shown in Fig. 8. The response is quite flat out to about 1GHz, but may then develop variations that are shown here as generic curves between 1GHz and 10GHz. The amplitude of these variations can be several dB, which represents a significant measurement error because it is uncertain where such variations will occur unless they are mapped to a lookup table.

However, by using two log amps in accordance with the present invention, and by designing the channel A and channel B log amps to have the same frequency response, the numerator and denominator of the function being measured suffer from the same variations. That is, V_A and V_B are each multiplied by h(s)•g(s), so their effects cancel:

$$V_{OUT} = V_y \log\left(\frac{V_A}{V_B} \cdot \frac{h(s) \cdot g(s)}{h(s) \cdot g(s)}\right) \qquad \text{(Eq. 6)}$$

Thus, instead of having a limited frequency range above which errors accumulate rapidly, the build-up of errors in the ratio measurement is deferred to a much higher frequency by virtue of cancellation of the independent frequency responses of the log amps, as well as the cancellation of the packaging parasitics.

Another advantage of the present invention relates to noise performance. In the case of the prior art log amp shown in Fig. 1, the noise voltage e_n figures into the output characteristic as follows:

$$V_{OUT} = V_y \log\left(\frac{V_{IN} + e_n}{V_x}\right) \qquad \text{(Eq. 7)}$$

As Vin approaches zero, there is a residual response due to noise generated in the log amps which is shown as the broken line in Fig. 3. In this region, measurement errors become large. However, with two log amps in accordance with the present invention, the noise affects the output as follows:

$$V_{OUT} = V_y \log\left(\frac{V_A + e_n}{V_B + e_n}\right) \qquad \text{(Eq. 8)}$$

If the noise voltages are well-matched (which is especially easy to achieve with co-integrated log amps), then when V_A and V_B are equally small, V_{OUT} is proportional to the log of one, which is zero, as it should be for equal signals of any amplitude, including very small signals. While not perfect, the reduction in measurement error is significant and of considerable practical value.

Having described and illustrated the principles of the invention in a preferred embodiment thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. I claim all modifications and variations coming within the spirit and scope of the following claims.

CLAIMS

1. A measurement system comprising:

a first log amp; and

a second log amp.

2. A measurement system according to claim 1 further comprising a differencing circuit coupled to the first and second log amps.

3. A measurement system according to claim 2 wherein:

the first log amp has a first logarithmic output coupled a first input to the differencing circuit; and

the second log amp has a second logarithmic output coupled to a second input to the differencing circuit.

4. A measurement system according to claim 3 wherein the differencing circuit comprises a summing node.

5. A measurement system according to claim 2 further comprising an output interface circuit coupled to the differencing circuit.

6. A measurement system according to claim 2 further comprising a phase detector core coupled to the first and second log amps.

7. A measurement system according to claim 6 wherein:

the first log amp has a first limiting output coupled to a first input of the phase detector core; and

the second log amp has a second limiting output coupled to a second input of the phase detector core.

8. A measurement system according to claim 7 wherein the detector core comprises a multiplier.

9. A measurement system according to claim 6 further comprising an output interface circuit coupled to the phase detector core.

10. A measurement system according to claim 1 wherein the first and second log amps are co-integrated on a substrate.

11. A measurement system according to claim 10 wherein the first and second log amps are arranged symmetrically about a center line.

12. A measurement system circuit according to claim 10 wherein the substrate is mounted in a package.

13. A measurement system according to claim 12 further comprising:

a first parasitic network coupled to the first log amp; and

a second parasitic network coupled to the second log amp;

wherein the first and second parasitic networks have similar frequency responses.

14. A measurement system according to claim 2 further comprising a third log amp coupled to the differencing circuit.

15. A measurement system according to claim 2 further comprising one or more additional log amps coupled to the differencing circuit.

16. A measurement system comprising:

a first log amp having a first limiting output;

a second log amp having a second limiting output; and

a phase detector core coupled to the first and second log amps to receive the first and second limiting outputs.

17. A measurement system according to claim 16 wherein the phase detector core comprises a multiplier.

18. A measurement system according to claim 16 wherein the first and second log amps are co-integrated on a substrate.

19. An integrated circuit comprising two or more log amps.

20. An integrated circuit according to claim 19 further comprising a differencing circuit coupled to the two or more log amps.

21. An integrated circuit according to claim 19 further comprising a phase detector core coupled to the two or more log amps.

22. A method comprising:

logarithmically amplifying a first input signal, thereby generating a first output signal;

logarithmically amplifying a second input signal, thereby generating a second output signal; and

differentially processing the first and second output signals.

23. A method according to claim 22 wherein:

the first and second output signals are logarithmic output signals; and

differentially processing the first and second output signals comprises differencing the first and second output signals.

24. A method according to claim 22 wherein:

the first and second output signals are limiting output signals; and

differentially processing the first and second output signals comprises multiplying the first and second output signals.

25. A method according to claim 22 further comprising:
utilizing a signal to be examined as the first input signal; and
utilizing a reference signal as the second input signal.

26. A method according to claim 25 wherein the reference signal has the same waveform as the signal to be examined.

27. A method according to claim 22 further comprising:
utilizing a modulated signal for the first input signal; and
utilizing a modulation signal for the second input signal.

ABSTRACT

A gain-phase detector differentially processes the outputs from two logarithmic amplifiers to provide ratiometric gain measurement, thereby eliminating intercept as a parameter. Hard-limited outputs from the dual amplifiers are multiplied in a logarithmic scalable phase detector core to provide a calibrated phase measurement output. In the preferred embodiment, two logarithmic amplifiers and other circuitry are co-integrated on a single substrate to provide a high degree of matching between the amplifiers, thereby canceling errors in the individual frequency responses of the individual amplifiers, extending the usable frequency response, and improving effective noise figure. Other numbers of logarithmic amplifiers can be used, and their various outputs can be added, subtracted, multiplied and combined in other manners to produce continuous products, continuous quotients, mixtures of products and quotients, etc., all of RF demodulated signals.

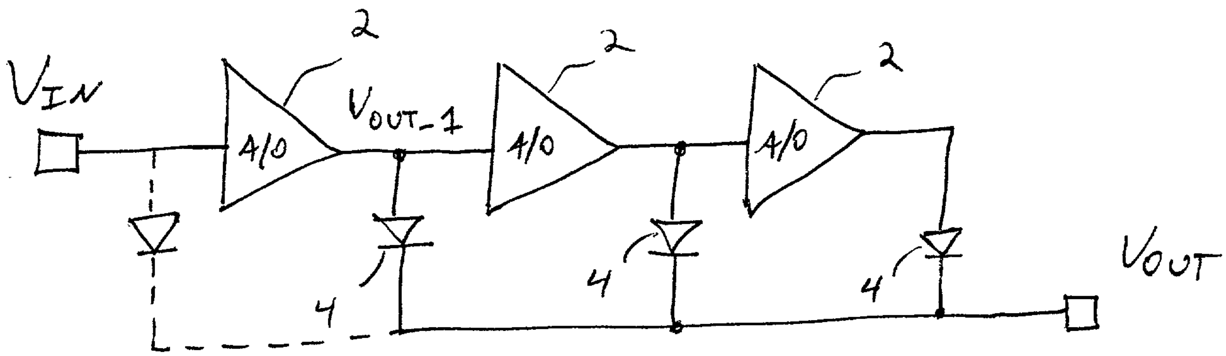

Fig. 1 (Prior Art)

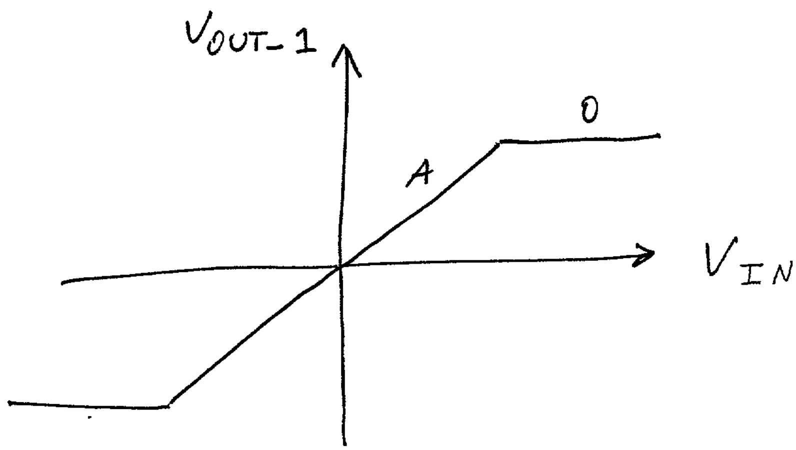

Fig. 2

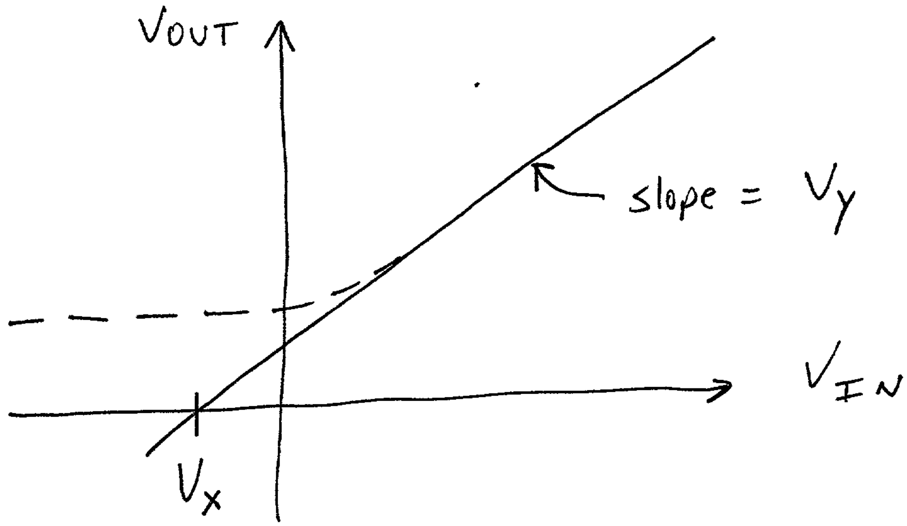

Fig. 3

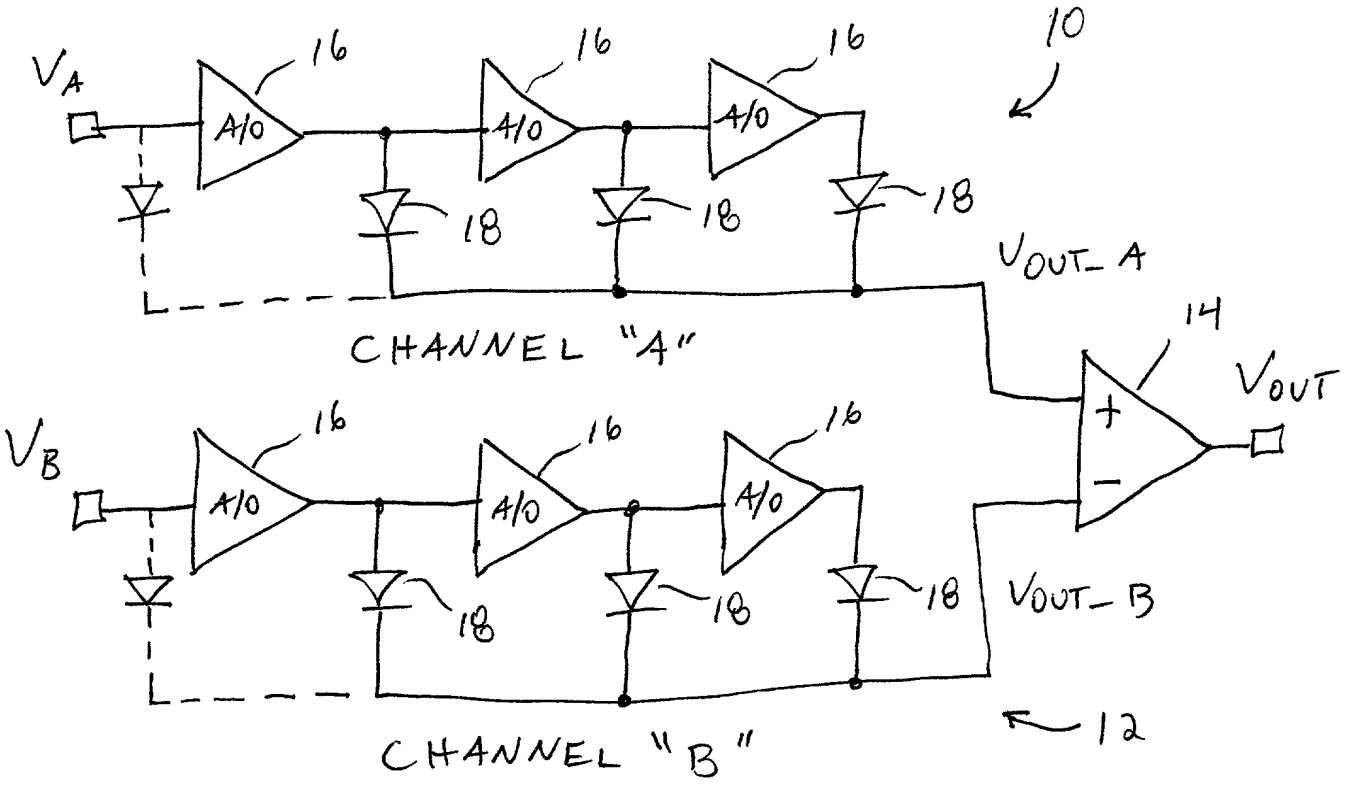
10
V_A
16
A/D
18
V_{OUT_A}
CHANNEL "A"
14
V_{OUT}
+
−
V_B
V_{OUT_B}
12
CHANNEL "B"

Fig. 4

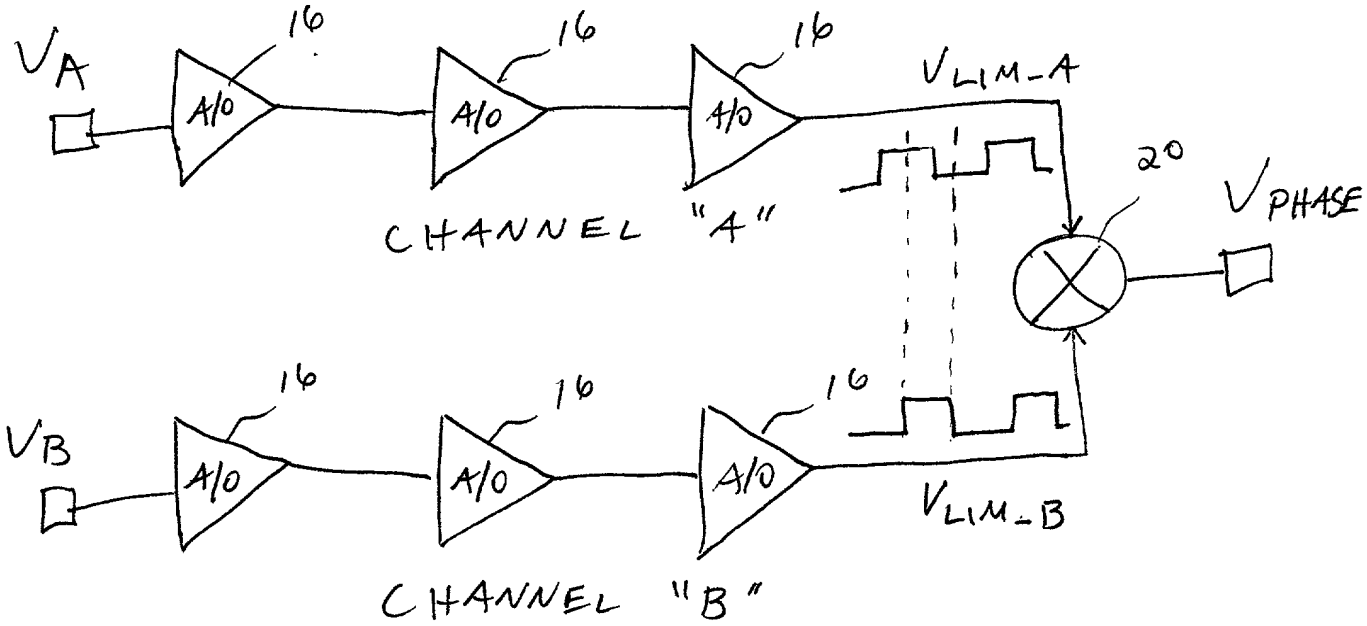
V_A
16
A/D
V_{LIM_A}
CHANNEL "A"
20
V_{PHASE}
V_B
V_{LIM_B}
CHANNEL "B"

Fig. 5

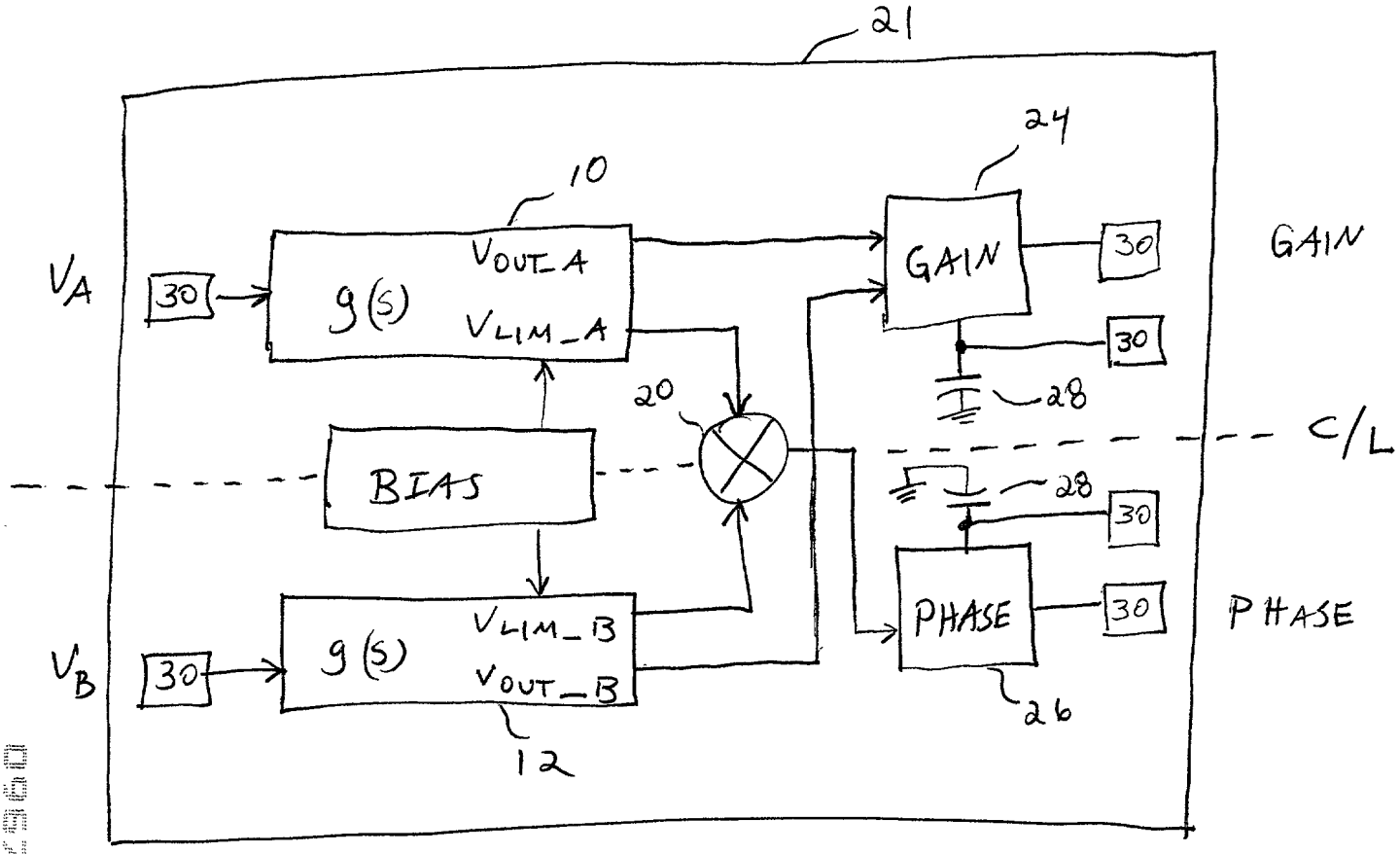
21
24
10
V_A
30
g(s)
V_{OUT_A}
V_{LIM_A}
GAIN
30
GAIN
30
28
20
C/L
BIAS
28
30
PHASE
30
PHASE
V_B
30
g(s)
V_{LIM_B}
V_{OUT_B}
26
12

Fig. 6

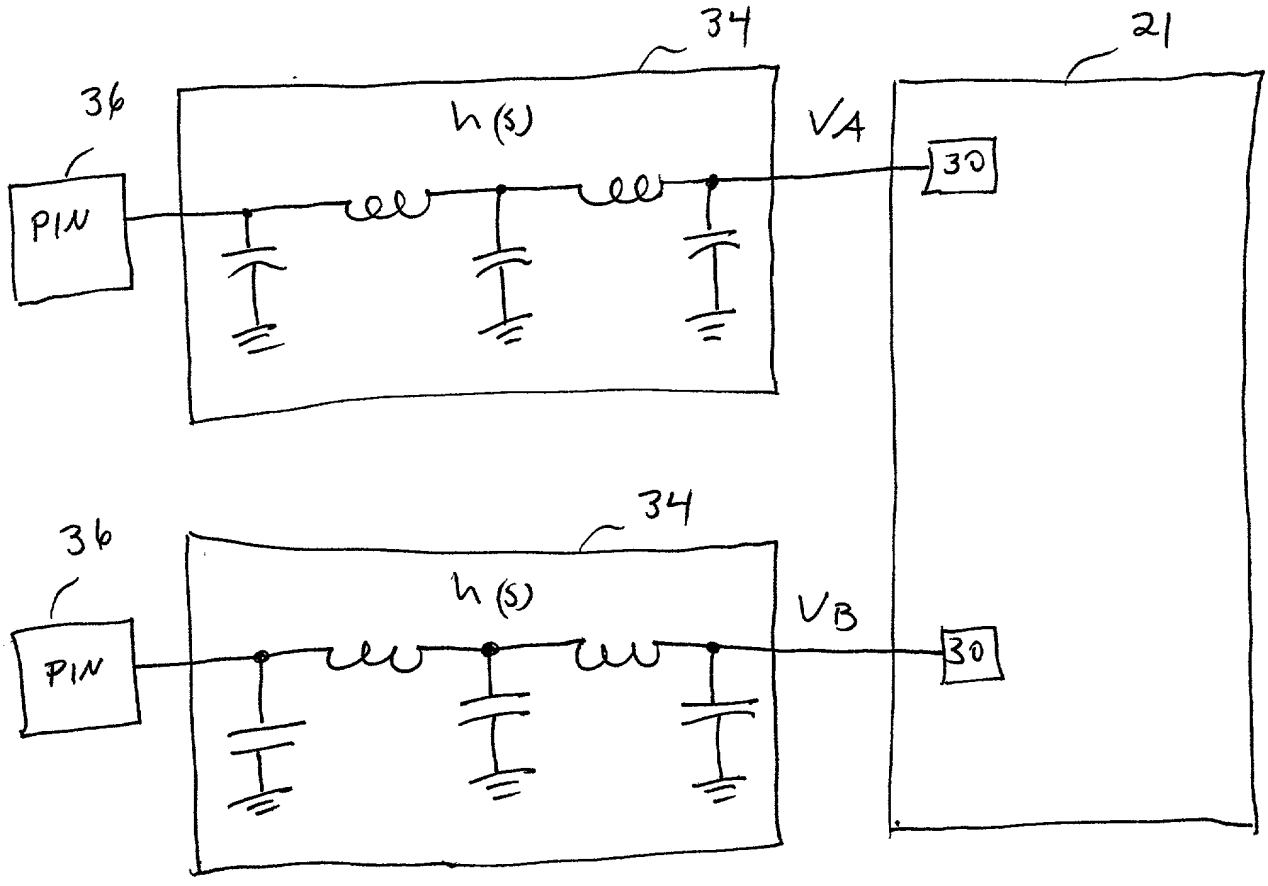
34
21
36
h(s)
V_A
PIN
30
34
36
h(s)
V_B
PIN
30

Fig. 7

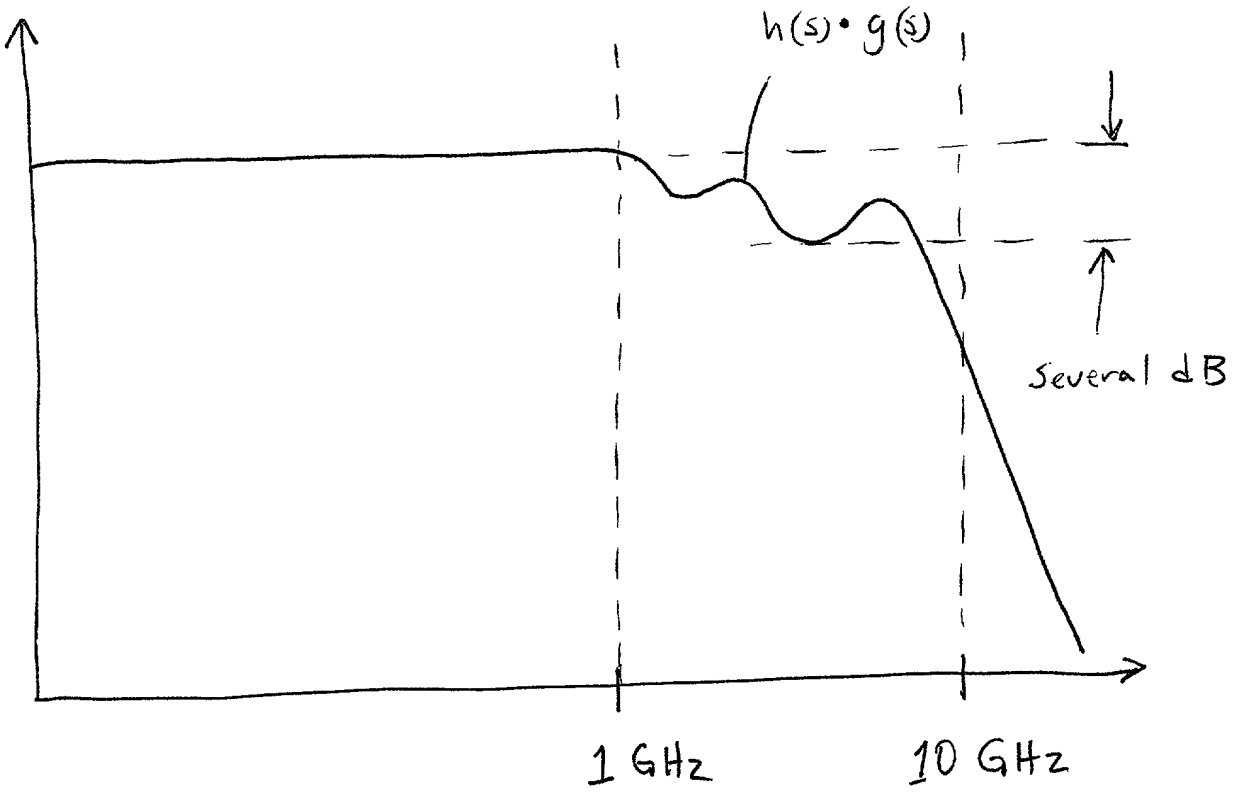

Fig. 8

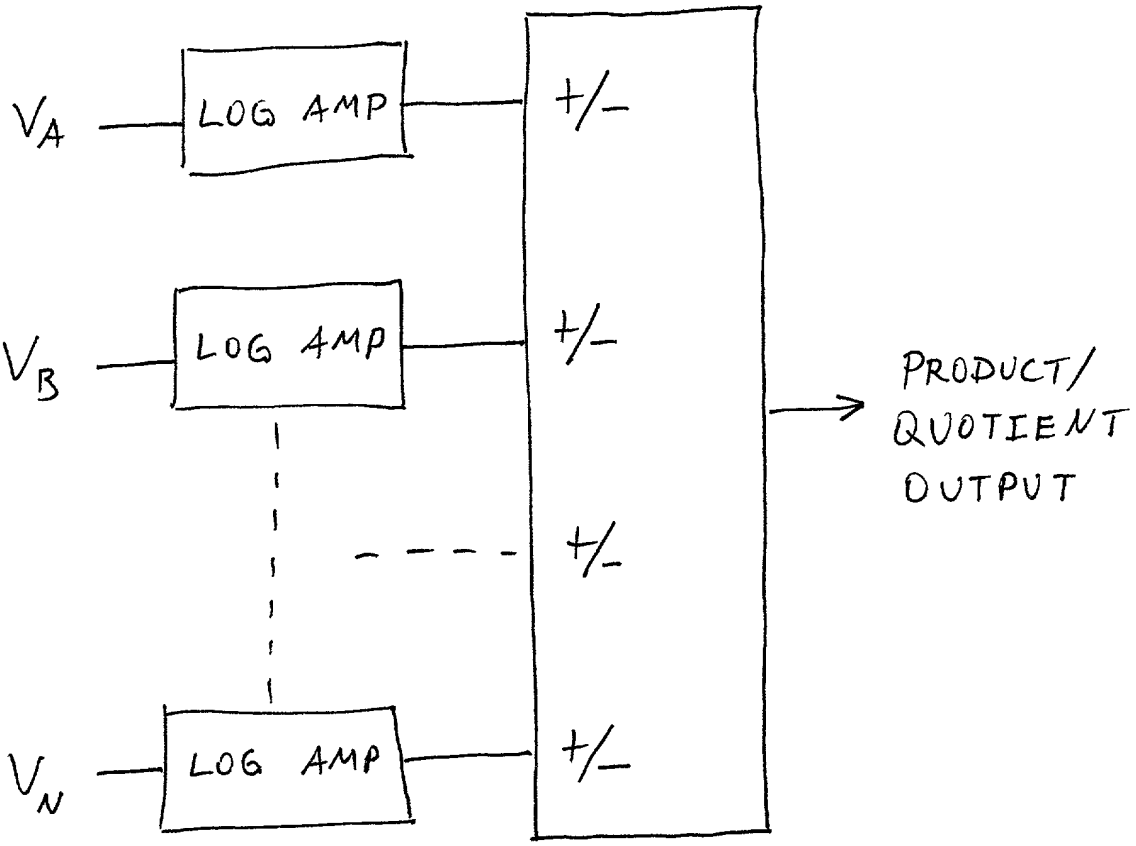

Fig. 9

PATENT APPLICATION
Attorney Docket No. 1482-129

COMBINED DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled GAIN AND PHASE DETECTOR HAVING DUAL LOGARITHMIC AMPLIFIERS, the specification of which:

[X] is attached hereto.
[ ] was filed on _____ as Application No. _____
[ ] and was amended on _____(if applicable)
[ ] with amendments through _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, Sec. 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Sec. 119 (a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Claiming Priority?	
(Number)	(Country)	(Day/Month/Year Filed)	[ ] Yes	[ ] No

I hereby claim the benefit under Title 35, United States Code, Sec. 119(e) of any United States provisional application listed below:

Provisional Application No.	Filing Date
60/231,505	September 9, 2000

I hereby claim the benefit under Title 35, United States Code, Sec. 120 or §365(c) of any PCT international application designating the United States of America listed below and,

insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Sec. 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Sec. 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorneys to prosecute the application, to file a corresponding international application, to prosecute and transact all business in the Patent and Trademark Office connected therewith:

Customer No. 20575

Attorney Name	Registration No.
Jerome S. Marger	26,480
Alexander C. Johnson, Jr.	29,396
Alan T. McCollom	28,881
James G. Stewart	32,496
Glenn C. Brown	34,555
Stephen S. Ford	35,139
Julie L. Reed	35,349
Gregory T. Kavounas	37,862
Scott A. Schaffer	38,610
Joseph S. Makuch	39,286
James E. Harris	40,013
Graciela G. Cowger	42,444
Ariel Rogson	43,054
Craig R. Rogers	43,888

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor: Barrie Gilbert

Inventor's signature: ______________________________ ____________

(Date)

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